WHAT IS CLAIMED IS:

1. An error and sync detection device, comprising:

a data rearrangement block for receiving 7-bit byte data and converting the 7-bit byte data to 8-bit byte data;

a parity check block for receiving the 8-bit byte data, which has been converted by the data rearrangement block, and performing an MPEG sync byte detection operation and a parity-check-based error detection operation using the received byte data; and

a data storage block, capable of receiving/outputting 8-bit byte data, for receiving and storing the 8-bit byte data, which has been converted by the data rearrangement block, and 8-bit intermediate byte data produced during a calculation process for the MPEG sync byte detection operation and the parity-check-based error detection operation performed by the parity check block,

whereby MPEG packet data that is a collection of 8-bit byte data including a sync byte is output from the parity check block.

2. The error and sync detection device of claim 1, wherein the data rearrangement block produces:

first 8-bit byte data that is obtained by combining preceding byte data with an upper 1 bit of following byte data, with the preceding byte data being 7-bit byte data and the following byte data being also 7-bit byte data that is received following the preceding byte data;

second 8-bit byte data that is obtained by combining lower 6 bits of the preceding byte data with upper 2 bits of following byte data; and

third to seventh 8-bit byte data that are obtained similarly by combining lower n bits (n=5, 4, 3, 2, 1) of the preceding byte data with upper m bits (m=3, 4, 5, 6, 7) of the following byte data.

3. The error and sync detection device of claim 1, wherein:

the parity check block includes a first calculation block and a second calculation block for performing a predetermined syndrome computation including an operation of delaying data by a predetermined number of clocks;

the first calculation block receives the 8-bit byte data that is output from the data rearrangement block, and performs a calculation therewith before the operation of delaying the data by a predetermined number of clocks, so as to output intermediate byte data to the data storage block, the intermediate byte data representing a result of the calculation; and

the second calculation block receives the intermediate byte data from the data storage block, and performs the calculation therewith before the operation of delaying the data by a predetermined number of clocks, so as to output 8-bit byte data that has undergone the MPEG sync byte detection operation and the parity-check-based error

detection operation.

4. The error and sync detection device of claim 3, wherein where pdatai[7:0] denotes input 8-bit byte data, gxot[7:0] denotes data representing a result of a calculation that is performed using the byte data pdatai[7:0], gxot7d[7:0] denotes 8-bit byte data obtained by delaying the calculation result data gxot[7:0] by 7 clocks according to a predetermined reference clock, gx[7:0] denotes an 8-bit intermediate variable that is used in a process of obtaining the calculation result data gxot[7:0], and "^" denotes an exclusive OR operation between bits,

the first calculation block calculates the respective bits gx[7], gx[6], gx[5], gx[4], gx[3], gx[2], gx[1] and gx[0] of the 8-bit intermediate variable gx[7:0] respectively by the following expressions:

gx[0]=gxot7d[0];

gx[1]=gxot7d[1];

gx[2]=gxot7d[2]^gxot7d[0];

gx[3]=gxot7d[3]^gxot7d[1]^gxot7d[0];

gx[4]=gxot7d[4]^gxot7d[2]^gxot7d[1];

gx[5]=gxot7d[5]^gxot7d[3]^gxot7d[2];

gx[6]=gxot7d[6]^gxot7d[4]^gxot7d[3]; and

gx[7]=gxot7d[7]^gxot7d[5]^gxot7d[4]^gxot7d[0], and

the first calculation block calculates the respective bits gxot[7], gxot[6], gxot[5], gxot[4], gxot[3], gxot[2], gxot[1] and gxot[0] of the calculation result data gxot[7:0]

respectively by the following expressions using the intermediate variable gx[7:0]:

```
gxot[7]=gx[7]^pdatai[7];
gxot[6]=gx[7]^gx[6]^pdatai[7]^pdatai[6];
gxot[5]=gx[7]^gx[6]^gx[5]
        ^pdatai[7]^pdatai[6]^pdatai[5];
gxot[4]=gx[7]^gx[6]^gx[5]^gx[4]
        ^pdatai[7]^pdatai[6]^pdatai[5]^pdatai[4];
gxot[3]=gx[7]^gx[6]^gx[5]^gx[4]^gx[3]
        ^pdatai[7]^pdatai[6]^pdatai[5]
        ^pdatai[4]^pdatai[3];
gxot[2]=gx[6]^gx[5]^gx[4]^gx[3]^gx[2]
        ^pdatai[6]^pdatai[5]^pdatai[4]
        ^pdatai[3]^pdatai[2];
gxot[1]=gx[5]^gx[4]^gx[3]^gx[2]^gx[1]
        ^pdatai[5]^pdatai[4]^pdatai[3]
        ^pdatai[2]^pdatai[1]; and
gxot[0]=gx[4]^gx[3]^gx[2]^gx[1]^gx[0]
        ^pdatai[4]^pdatai[3]^pdatai[2]
        ^pdatai[1]^pdatai[0].
```

5. The error and sync detection device of claim 3, wherein where dobx[7:0] denotes input 8-bit byte data, bxot1[7:0] denotes data representing a result of a calculation that is performed using the byte data dobx[7:0], dobx7d[7:0] denotes 8-bit byte data obtained by delaying the input byte data dobx[7:0] by 7 clocks according to a

predetermined reference clock, bx[7:0] denotes an 8-bit intermediate variable that is used in a process of obtaining the calculation result data bxot1[7:0], gxot1d[7:0] denotes 8-bit byte data obtained by delaying the calculation result data gxot[7:0] from the first calculation block by 1 clock according to the reference clock, and "^" denotes an exclusive OR operation between bits,

the second calculation block calculates the respective bits bx[7], bx[6], bx[5], bx[4], bx[3], bx[2], bx[1] and bx[0] of the 8-bit intermediate variable bx[7:0] respectively by the following expressions:

```
bx[0]=dobx7d[0];
bx[1]=dobx7d[1];
bx[2]=dobx7d[2];
bx[3]=dobx7d[3];
bx[4]=dobx7d[4];
bx[5]=dobx7d[5]^dobx[1];
bx[6]=dobx7d[6]^dobx[2]; and
bx[7]=dobx7d[7]^dobx[3]^dobx[1],
```

the second calculation block calculates the respective bits bxot1[7], bxot1[6], bxot1[5], bxot1[4], bxot1[3], bxot1[2], bxot1[1] and bxot1[0] of the calculation result data bxot1[7:0] respectively by the following expressions:

```
bxot1[7]=bx[7]^dobx[0];
bxot1[6]=bx[6]^bx[0]^dobx[7];
```

bxot1[5]=bx[5]^dobx[7]^dobx[6];

bxot1[4]=bx[4]^bx[0]^dobx[6]^dobx[5];

bxot1[3]=bx[3]^dobx[7]^dobx[5]^dobx[4];

bxot1[2]=bx[2]^dobx[6]^dobx[4]^dobx[3];

bxot1[1]=bx[1]^dobx[5]^dobx[3]^dobx[2]; and

bxot1[0]=bx[0]^dobx[4]^dobx[2]^dobx[1], and

the second calculation block calculates 8-bit byte data bxot2[7:0], representing a result of a calculation that is performed based on the calculation result data bxot1[7:0] and the calculation result data gxot[7:0] from the first calculation block, by the following expression:

bxot2[7:0]=bxot1[7:0]^gxot1d[7:0].

6. The error and sync detection device of claim 3, wherein the data storage block receives the 8-bit byte data from the data rearrangement block and 8-bit byte data representing the result of the calculation performed by the first calculation block, and outputs the two 8-bit byte data after holding the two 8-bit byte data respectively for predetermined periods of time.

7. The error and sync detection device of claim 1, wherein the data storage block is a RAM.

8. An error and sync detection method, comprising:

a data rearrangement step of receiving 7-bit byte data and converting the 7-bit byte data to 8-bit byte data; and

a parity check step of receiving the 8-bit byte data,

which has been converted in the data rearrangement step, performing a syndrome calculation using the received byte data, temporarily storing 8-bit intermediate byte data produced during the calculation process in a data storage device, and continuing to perform the syndrome calculation using the intermediate byte data stored in the data storage device, thus performing an MPEG sync byte detection operation and a parity-check-based error detection operation,

whereby MPEG packet data that is a collection of 8-bit byte data including a sync byte is output.

9. The error and sync detection method of claim 8, wherein the data rearrangement step includes the step of producing:

first 8-bit byte data that is obtained by combining preceding byte data with an upper 1 bit of following byte data, with the preceding byte data being 7-bit byte data and the following byte data being also 7-bit byte data that is received following the preceding byte data;

second 8-bit byte data that is obtained by combining lower 6 bits of the preceding byte data with upper 2 bits of following byte data; and

third to seventh 8-bit byte data that are obtained similarly by combining lower n bits (n=5, 4, 3, 2, 1) of the preceding byte data with upper m bits (m=3, 4, 5, 6, 7) of the following byte data.

10. The error and sync detection method of claim 8,

wherein:

the parity check step includes a first calculation step and a second calculation step for performing a predetermined syndrome computation including an operation of delaying data by a predetermined number of clocks;

the first calculation step includes the step of receiving the 8-bit byte data, which has been converted in the data rearrangement step, and performing a calculation therewith before the operation of delaying the data by a predetermined number of clocks, so as to output 8-bit intermediate byte data to the data storage device, the 8-bit intermediate byte data representing a result of the calculation; and

the second calculation step includes the step of receiving the intermediate byte data from the data storage device, and performing the calculation therewith before the operation of delaying the data by a predetermined number of clocks, so as to output 8-bit byte data that has undergone the MPEG sync byte detection operation and the parity-check-based error detection operation.

11. The error and sync detection method of claim 10,

wherein in the first calculation step, where pdatai[7:0] denotes input 8-bit byte data, gxot[7:0] denotes data representing a result of a calculation that is performed using the byte data pdatai[7:0], gxot7d[7:0] denotes 8-bit byte data obtained by delaying the calculation result data

gxot[7:0] by 7 clocks according to a predetermined reference clock, gx[7:0] denotes an 8-bit intermediate variable that is used in a process of obtaining the calculation result data gxot[7:0], and "^" denotes an exclusive OR operation between bits,

the respective bits gx[7], gx[6], gx[5], gx[4], gx[3], gx[2], gx[1] and gx[0] of the 8-bit intermediate variable gx[7:0] are calculated respectively by the following expressions:

```
gx[0]=gxot7d[0];
gx[1]=gxot7d[1];
gx[2]=gxot7d[2]^gxot7d[0];
gx[3]=gxot7d[3]^gxot7d[1]^gxot7d[0];
gx[4]=gxot7d[4]^gxot7d[2]^gxot7d[1];
gx[5]=gxot7d[5]^gxot7d[3]^gxot7d[2];
gx[6]=gxot7d[6]^gxot7d[4]^gxot7d[3]; and
gx[7]=gxot7d[7]^gxot7d[5]^gxot7d[4]^gxot7d[0], and
```

the respective bits gxot[7], gxot[6], gxot[5], gxot[4], gxot[3], gxot[2], gxot[1] and gxot[0] of the calculation result data gxot[7:0] are calculated respectively by the following expressions using the intermediate variable gx[7:0]:

```
gxot[7]=gx[7]^pdatai[7];
gxot[6]=gx[7]^gx[6]^pdatai[7]^pdatai[6];
gxot[5]=gx[7]^gx[6]^gx[5]
        ^pdatai[7]^pdatai[6]^pdatai[5];
```

```
gxot[4]=gx[7]^gx[6]^gx[5]^gx[4]
        ^pdatai[7]^pdatai[6]^pdatai[5]^pdatai[4];
gxot[3]=gx[7]^gx[6]^gx[5]^gx[4]^gx[3]
        ^pdatai[7]^pdatai[6]^pdatai[5]
        ^pdatai[4]^pdatai[3];
gxot[2]=gx[6]^gx[5]^gx[4]^gx[3]^gx[2]
        ^pdatai[6]^pdatai[5]^pdatai[4]
        ^pdatai[3]^pdatai[2];
gxot[1]=gx[5]^gx[4]^gx[3]^gx[2]^gx[1]
        ^pdatai[5]^pdatai[4]^pdatai[3]
        ^pdatai[2]^pdatai[1]; and
gxot[0]=gx[4]^gx[3]^gx[2]^gx[1]^gx[0]
        ^pdatai[4]^pdatai[3]^pdatai[2]
        ^pdatai[1]^pdatai[0].
```

12. The error and sync detection method of claim 10, wherein in the second calculation step, where dobx[7:0] denotes input 8-bit byte data, bxot1[7:0] denotes data representing a result of a calculation that is performed using the byte data dobx[7:0], dobx7d[7:0] denotes 8-bit byte data obtained by delaying the input byte data dobx[7:0] by 7 clocks according to a predetermined reference clock, bx[7:0] denotes an 8-bit intermediate variable that is used in a process of obtaining the calculation result data bxot1[7:0], gxot1d[7:0] denotes 8-bit byte data obtained by delaying the calculation result data gxot[7:0] from the first calculation step by 1 clock according to the reference clock, and "^"

denotes an exclusive OR operation between bits,

the respective bits bx[7], bx[6], bx[5], bx[4], bx[3], bx[2], bx[1] and bx[0] of the 8-bit intermediate variable bx[7:0] are calculated respectively by the following expressions:

```
bx[0]=dobx7d[0];
bx[1]=dobx7d[1];
bx[2]=dobx7d[2];
bx[3]=dobx7d[3];
bx[4]=dobx7d[4];
bx[5]=dobx7d[5]^dobx[1];
bx[6]=dobx7d[6]^dobx[2]; and
bx[7]=dobx7d[7]^dobx[3]^dobx[1],
```

the respective bits bxot1[7], bxot1[6], bxot1[5], bxot1[4], bxot1[3], bxot1[2], bxot1[1] and bxot1[0] of the calculation result data bxot1[7:0] are calculated respectively by the following expressions:

```
bxot1[7]=bx[7]^dobx[0];
bxot1[6]=bx[6]^bx[0]^dobx[7];
bxot1[5]=bx[5]^dobx[7]^dobx[6];
bxot1[4]=bx[4]^bx[0]^dobx[6]^dobx[5];
bxot1[3]=bx[3]^dobx[7]^dobx[5]^dobx[4];
bxot1[2]=bx[2]^dobx[6]^dobx[4]^dobx[3];
bxot1[1]=bx[1]^dobx[5]^dobx[3]^dobx[2]; and
bxot1[0]=bx[0]^dobx[4]^dobx[2]^dobx[1], and
```

8-bit byte data bxot2[7:0], representing a result of

a calculation that is performed based on the calculation result data bxot1[7:0] and the calculation result data gxot[7:0] from the first calculation step, is calculated by the following expression:

bxot2[7:0]=bxot1[7:0]^gxot1d[7:0].

13. The error and sync detection method of claim 10, wherein the parity check step includes the steps of:

storing 8-bit byte data successively passed from the data rearrangement step to the first calculation step in the data storage device, and holding the 8-bit byte data in the data storage device for a predetermined period of time;

storing 8-bit byte data representing a result of a calculation in the first calculation step in the data storage device; and

passing the 8-bit byte data representing the result of the calculation in the first calculation step from the data storage device to the second calculation step after holding the 8-bit byte data in the data storage device for the predetermined period of time.